Research presentation
NoC Emulation

Nicolas Genko EPFL/LSI

David Atienza UCM/CACYA

Outline

- NoC Emulation with NIs

- Visual application of NoC on FPGA
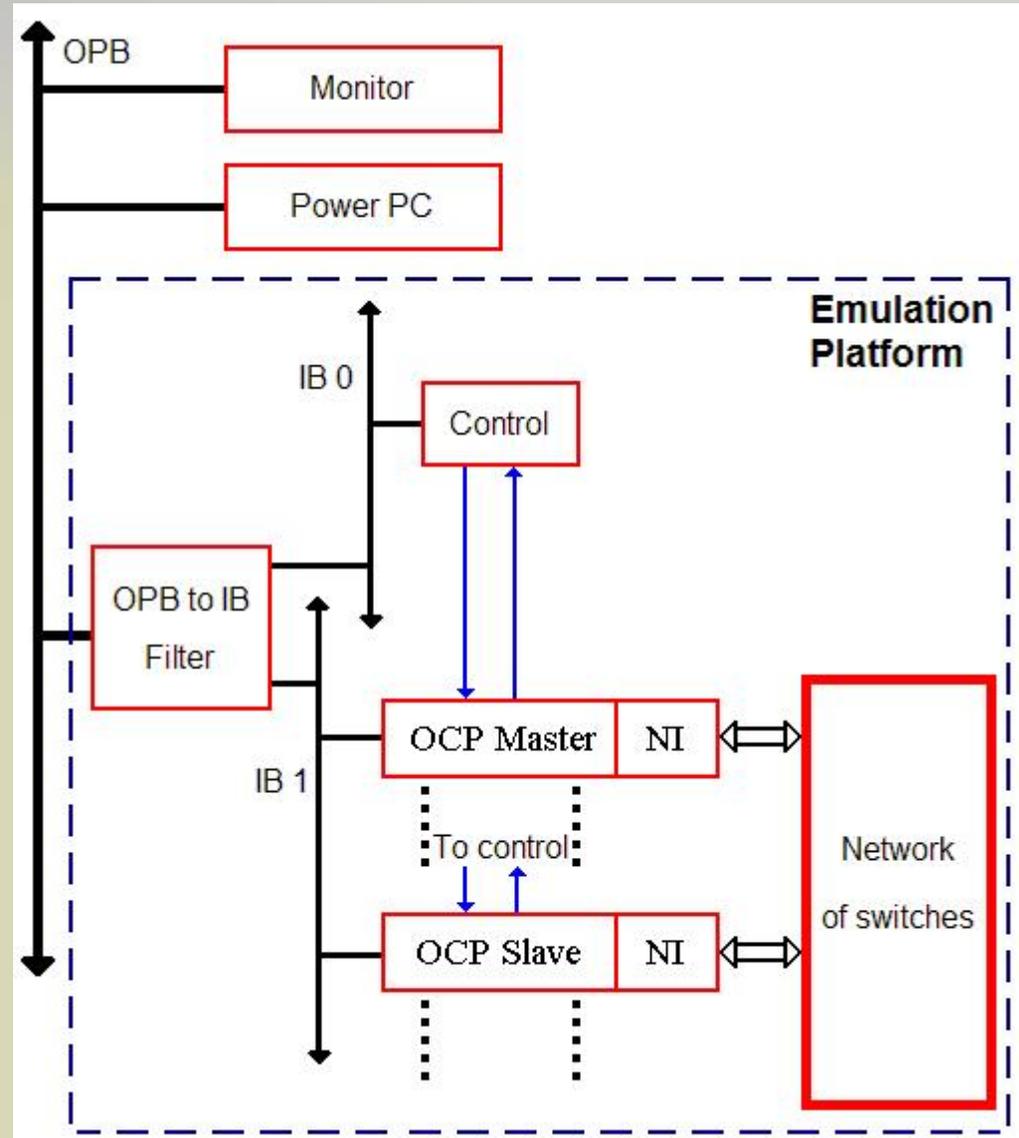
- Status of current work

Emulation Platform which include NIs

- Emulation platform based on the previous emulation scheme.
- Two types of traffic devices.
  - Programmable OCP master cores.
    - Those cores generate traffic (trace driven or stochastic) as previous TG did.
    - It analyzes the received traffic as previous TR did.
  - Memories which behave like any OCP slave device.
    - Also programmable.
    - For example, programmable answer delay.
    - The memory can be scan by the system processor.

Platform with NIs: Figure

Platform presented
at DATE 05.

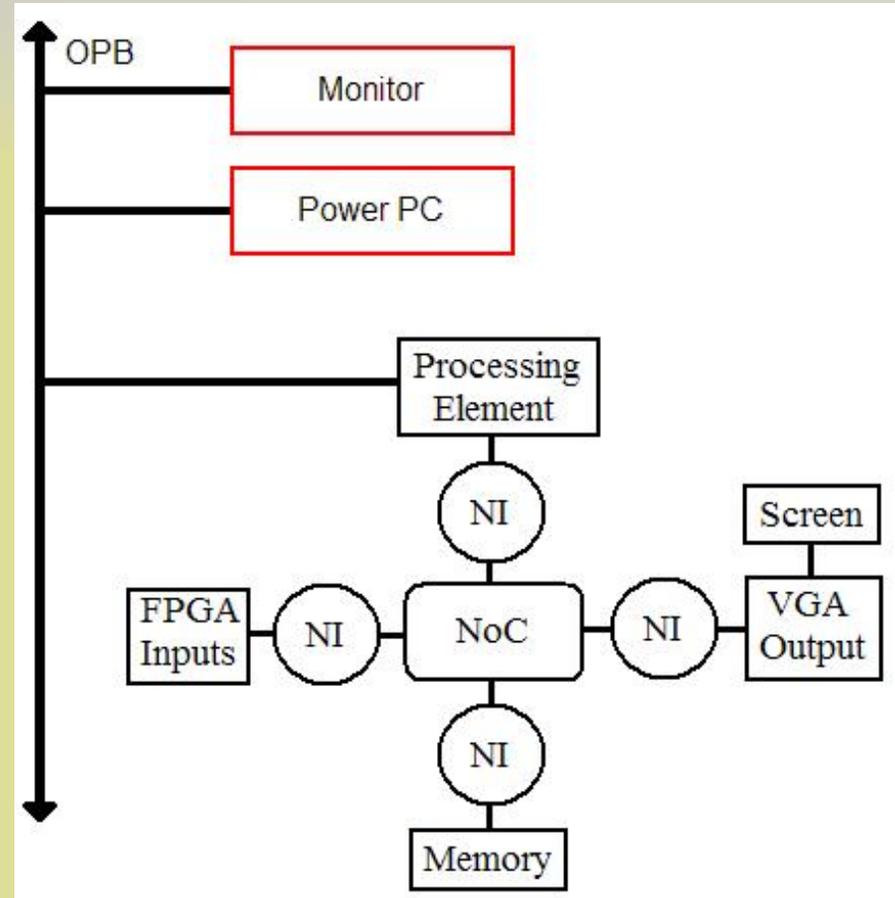Platform with NIs.

Outline

- NoC Emulation with NIs

- Visual application of NoC on FPGA

- Status of current work

Visual application of NoC

- The processor initializes the system.

- A monitor for debug and control purposes.

- A visual system which uses a NoC.

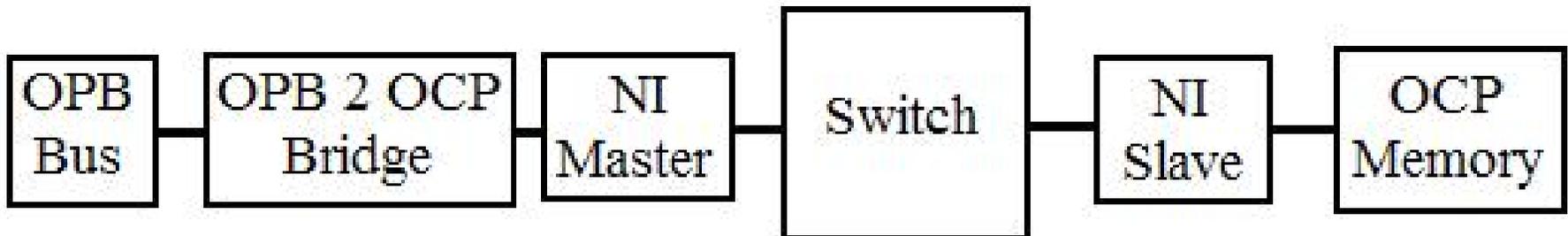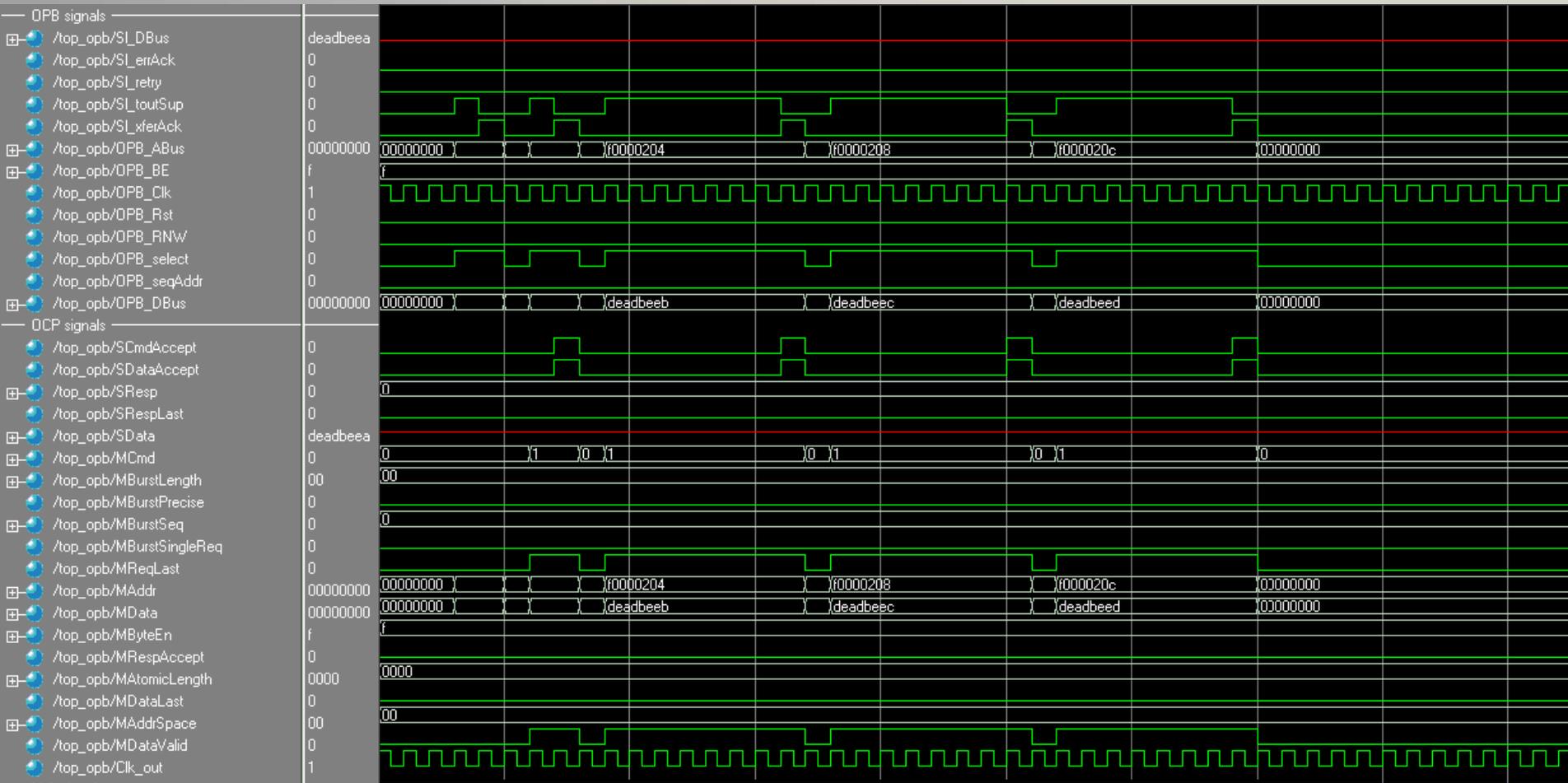- Could be extended to a MPEG decoder which uses a NoC.

Outline

- NoC Emulation with NIs

- Visual application of NoC on FPGA

- Status of current work
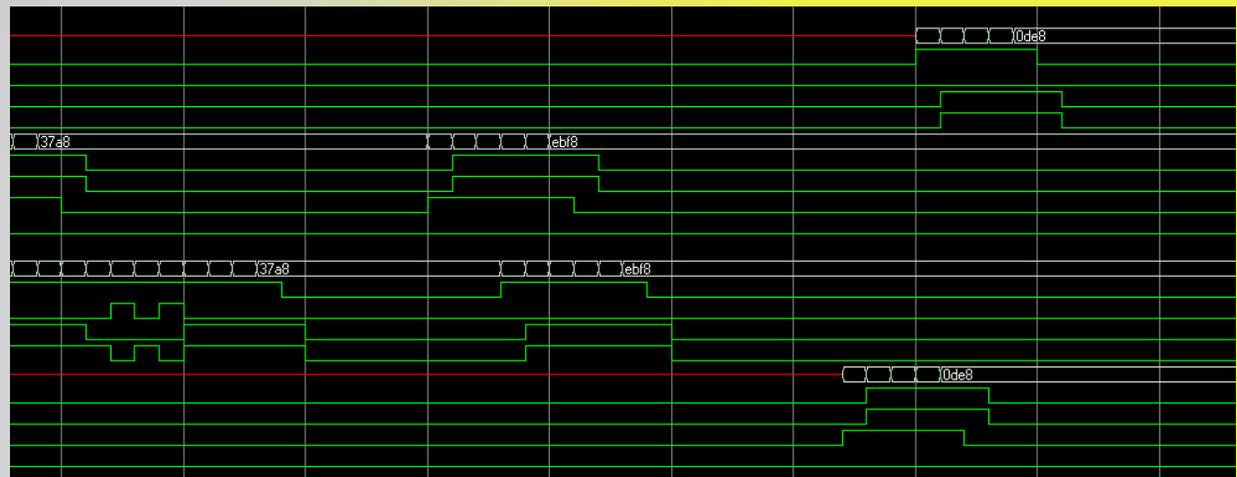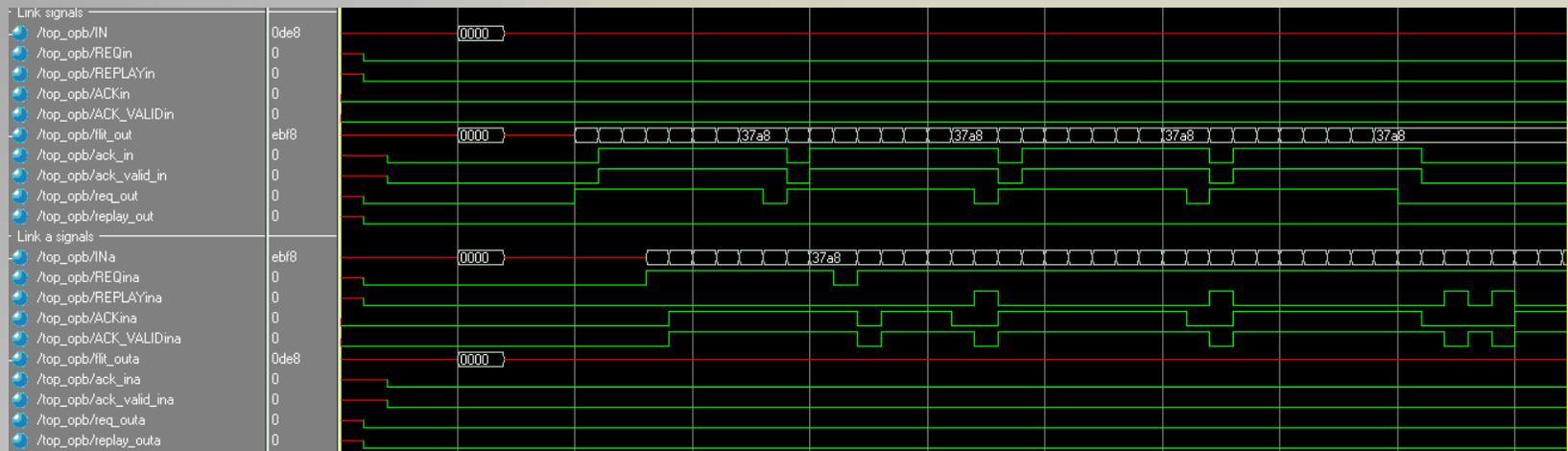
Status of current work

- Simulation of a NoC (switch + NIs) (November version) on Modelsim.

- OPB2OCP Bridge functional in its simple version.

- Possibility to plug a processor (PPC or µBlaze) on a NoC.

- The whole system is synthesizable.

OPB Bus — OPB 2 OCP Bridge — NI Master — Switch — NI Slave — OCP Memory

Status of current work

Status of current work

Conclusion

- Development of an emulation platform which includes NIs.

- An application which uses a NoC:
  - A first concrete project: a visual application which could be extended by a MPEG decoder.
  - A possible MPSoC on FPGA thanks to a OPB to OCP bridge.